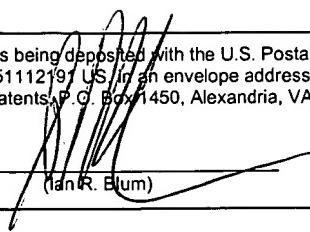




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whereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV 451112191 US in an envelope addressed to MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: February 8, 2006 Signature: 
(Ian R. Blum)

Docket No.: U2054.0107

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Patent Application of:
Junji Tajime et al.

Application No.: 09/334,354

Confirmation No.: 5240

Filed: June 16, 1999

Art Unit: 2613

For: MOVING PICTURE DECODING
APPARATUS AND MOVING PICTURE
DECODING METHOD

Examiner: R. J. Lee

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit this reply to the Examiner's Answer to specifically address the Examiner's grounds for rejection and response to arguments set forth in Sections 9 and 10, respectively.

1. The Examiner's grounds for rejection are incorrect.

In Section 9, paragraph 2 of the Examiner's grounds for rejection, the Examiner states that "the claimed limitations that constitute as new matter (see above paragraph (2)) have not been considered in the following rejections."

Appellants point out that the new matter rejections were withdrawn by the Examiner in the Advisory action dated July 8, 2005. Appellants believe this statement in the Examiner's answer was in error due to copying and pasting the rejection from the

Final Office Action, mailed April 1, 2005. See Final Office Action, mailed April 1, 2005, page 5.

In restating the rejection of claims 1-14 and 16-18 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,689 ("Ohira"), the Examiner's again equates the memory 103 of Ohira with the claimed "memory access unit". As previously argued, Appellants respectfully disagree with the Examiner's reasoning for equating Appellants' claimed "memory access unit" with the size of the memory.

The number of bits of the memory a cited in Ohira is unrelated to the number of bits of the memory access unit as claimed. In other words, memory size is not the memory bus (the memory access unit) that accesses the memory.

Appellants even provided the analogy that the storage capacity of a frame memory is equivalent to the parking spaces in a garage structure whereas the memory access unit is equivalent to the entrance ramp for the garage. However, even after providing this analogy, the Examiner notes that the storage capacity of the frame memory in Ohira is equivalent of a memory access unit of the memory. See Answer at page 9.

Due to the Examiner's misunderstanding that the memory access unit differs from the size of the memory, the pending claims have been continuously rejected. The Examiner's rejection is incorrect as discussed in the Appellants' Appeal Brief and Appellants respectfully request that the Board order the withdrawal of the Examiner's rejections.

2. Appellants arguments for patentability only address explicitly recited claimed limitations.

In the Examiner's response to arguments, Section 10 of the Examiner's Answer, the Examiner states that "the memory bus feature, as argued, is not even

claimed." See Answer at page 8. The Examiner further states that the memory bus feature arguments "do not correspond or correlate with the claim language. Put simply, these features are not claimed. Applicants respectfully disagree.

Claim 1 for example requires

a memory access width controller that controls said quantization controller such that bit allocation is controlled in relation to a number of bits of a memory access unit of said memory.

The plain meaning of this limitation is clearly: 1) that the memory access unit is something other than the memory; and 2) that the memory access unit is used to access the memory. Beyond the plain meaning of the words used in the claim, the entire specification makes it clear that the memory access unit is the bus used for accessing the memory.

The arguments raised by the Examiner that memory bus features of the invention are not claimed are therefore untenable. Appellants respectfully submit that it could not be clearer that such features are claimed. Appellants have addressed this memory access unit issue several times. See, Response to Non-Final Office Action dated December 24, 2003, pages 3-5; Amendment in Response to Non-Final Office Action dated October 20, 2004, pages 8-12; Amendment After Final Action dated June 15, 2005, pages 8-9. Appellants have repeatedly stated that the terms "memory bus" and "memory access unit" are interchangeable and that the term "memory bus" is the commonly used term for "memory access unit." See Id. Therefore, the arguments presented in Appellants' Appeal Brief, and other filings, only address explicitly recited claim limitations.

Appellants respectfully submit that the Board should order the Examiner's rejections withdrawn so that the pending case will issue.

Dated: February 8, 2006

Respectfully submitted,

By _____
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